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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/668,582	09/23/2003	Alfred Stufflet	I-2-0391.1US	2412

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EXAMINER	
MALEK, LEILA	

ART UNIT	PAPER NUMBER
2611	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

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Office Action Summary	Application No.	Applicant(s)	
	10/668,582	STUFFLET ET AL.	
	Examiner	Art Unit	
	Leila Malek	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 January 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-23 and 25-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-7,9-18,20-23,25-32 and 34-36* is/are rejected.

7)☒ Claim(s) *8,19 and 33* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09/23/2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Applicant's submission field on 01/11/2008 has been entered and the finality of the previous Office action has been withdrawn.

Claim Objections

2. Claim 27 is objected to because of the following informalities: claim 27, depends on claim 24, which has been canceled. Appropriate correction is required.

3. Claim 13 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of claim 12. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 7, 18, and 32 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. As to the above claims, limitation, the serial bus processor includes an output port configured to provide at least one of IBus, PBus, and/or RBus, is vague.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 23, 25, 26, 31, 34, 35, and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Phillips et al. (hereafter, referred as Phillips) (US 5,859,878), and Park et al. (hereafter, referred as Park) (US 6,373,902) further in view of Fischer et al. (hereafter, referred as Fischer) (US 5,768,695).

As to claim 23, Phillips discloses a digitally programmable transmit module 102 in a radio device (see Fig. 1) including an analog sub-module and a digital processing sub-module. Phillips further shows (see Fig. 1) that in the programmable common transmit module 102, the analog sub-module 108 and the digital sub-module 110 are connected through a tune bus processor 117. Phillips also shows an antenna interface processor 103 (interpreted as radio interface processor), which has been coupled to the serial tune bus processor 117 (through the analog sub-module). Phillips discloses all the subject matters claimed in claim 23, except for a plurality of lookup tables which are indexed by data received from the analog radio module; wherein the data values retrieved from the plurality of lookup tables may be used to generate processed data for controlling the digital module. Park discloses a device for linearizing a transmitter in a digital radio communication system (See the abstract). Park further discloses a plurality of lookup tables (See Fig. 3, blocks 351 and 353, and column 6, lines 5-9), which are indexed (as the I-channel pre-distortion look-up table and Q-channel pre-

distortion lookup table) by data received from the analog radio module (See Fig. 3 and column 3, lines 50-57); wherein the serial bus processor receives data from the plurality of lookup tables (see Fig. 2, wherein the baseband filters receive the compensated value from the analog part of the transmitter), and uses data values retrieved from the lookup tables to generate processed data for controlling the digital module (See Fig. 2). It would have been obvious to one of ordinary skill in the art at the time of invention to modify Phillips as suggested by Park to compensate for the non-linearties of the analog signal (see the abstract) and as the result increase the performance of the transmitter. Phillips and Park disclose all the limitations claimed in claim 23, except that the radio interface processor includes at least one memory-mapped register. Fischer, in the same field of endeavor, discloses an apparatus for providing a flexible interface for creating the necessary control signaling of a radio transmitter (see column 1, first paragraph). Fischer, further discloses a radio interface unit 402 (see Fig. 3), which includes a register set 406, which is coupled to the state machine 404 (See column 4, lines 27-39). Since the radio interface unit is a control device, which controls the elements that are connected to it, it would have been obvious to one of ordinary skill in the art at the time of invention to modify the Phillips' radio/antenna interface unit as suggested by Fischer to include the registers inside the radio interface device in order to save the control information of the other units. Fischer is silent in disclosing that the registers are memory-mapped registers, however since the memory-mapped registers have the fastest mechanism for data retrieval (e.g. as evidence by Santos et al. (US 5,933,158. see column 24, first paragraph)), it would

have been obvious to one of ordinary skill in the art at the time of invention to use these kind of registers instead of the registers used by Fischer for the reasons stated above.

As to claim 25, Park further discloses that the lookup tables are programmed with data so as to compensate for one or more nonlinearities which may be present in the analog radio module (See column 5, last paragraph, i.e. the signal has been converted to analog before calculating the distortion (therefore the distortions are related to the analog signal).

As to claim 26, Park further discloses that the serial bus processor receives data from the plurality of lookup tables (See Fig. 2, wherein the baseband filters receive the compensated value from the analog part of the transmitter), and uses data values retrieved from the lookup tables to generate processed data for controlling the digital module (See Fig. 2).

As to claim 31, Phillips further discloses a clock, coupled to the RIP, for determining the relative timing of external events, and also for controlling the analog radio module (See column 14, lines 35-49).

As to claim 34, Philips discloses that the RIP accessed controlling software that is programmed according to one or more specific electronic characteristics of a given analog audio module (see column 25, lines 14-20).

As to claim 35, Park discloses that the nonlinearities include at least one of AGC (automatic gain control) line voltage as a function of gain, and power level control voltage as a function of power output (See Fig. 3, blocks 217 and 223, and column 6,

lines 49-51), whereby the digital module need not be modified to work with the specific characteristics of a given analog radio module (i.e. the analog signal nonlinearities have been compensate before the transmission of signal to the digital module (see Figs. 5 and 6).

As to claim 36, Phillips discloses that the digital module is a time-division-duplex (see column 23, lines 8 and Fig. 1 for duplexing), user-equipment (See column 7, lines 47-55), application-specific-integrated-circuit (ASIC) (see column 14, lines 50-67).

6. Claims 1, 3, 4, 6, 9-15, 17, 20- 22, and 27-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Phillips, Park, and Fischer, further in view of Yarch et al. (hereafter, referred as Yarch) (US 5,761,532).

As to claims 1, 12, and 13 Phillips discloses a digitally programmable transmit module 102 in a radio device, including an analog sub-module and a digital processing sub-module (see Fig. 1). Phillips further shows that in the programmable common transmit module 102, the analog sub-module 108 and the digital sub-module 110 are connected through a tune bus processor 117. Phillips also shows an antenna interface processor 103 (interpreted as radio interface processor), which has been coupled to the serial tune bus processor 117 (through the analog sub-module). Phillips discloses all the subject matters claimed in claims 1, 12, and 13, except that the radio interface processor includes at least one memory-mapped register configured to control data generated by the serial bus processor. Phillips also does not disclose a plurality of lookup tables which are indexed by data received from the analog radio module, and which are programmed with data so as to compensate for one or more nonlinearities

which may be present in the analog radio module, but are not accounted for in the digital module; wherein the serial bus processor receives data from the plurality of lookup tables, and uses data values retrieved from the lookup tables to generate processed data for controlling the digital module. Park discloses a device for linearizing a transmitter in a digital radio communication system (see the abstract). Park further discloses a plurality of lookup tables (see Fig. 3, blocks 351 and 353, and column 6, lines 5-9) which are indexed (as the I-channel pre-distortion look-up table and Q-channel pre-distortion lookup table) by data received from the analog radio module (see Fig. 3 and column 3, lines 50-57), and which are programmed with data so as to compensate for one or more nonlinearities which may be present in the analog radio module (see column 5, last paragraph, i.e. the signal has been converted to analog before calculating the distortion; therefore the distortions are related to the analog signal); wherein the serial bus processor receives data from the plurality of lookup tables (see Fig. 2, wherein the baseband filters receive the compensated value from the analog part of the transmitter), and uses data values retrieved from the lookup tables to generate processed data for controlling the digital module (see Fig. 2). It would have been obvious to one of ordinary skill in the art at the time of invention to modify Phillips as suggested by Park to compensate for the non-linearties of the analog signal (See the abstract) and increase the performance of the transmitter. Phillips and Park disclose all the limitations claimed in claims 1, 12, and 13 except that the radio interface processor includes at least one memory-mapped register configured to control data generated by the serial bus processor. Fischer, in the same field of endeavor, discloses an apparatus

for providing a flexible interface for creating the necessary control signaling of a radio transmitter (see column 1, first paragraph). Fischer, further discloses a radio interface unit 402 (see Fig. 3), which includes a register set 406, which is coupled to the state machine 404 (see column 4, lines 27-39). Since the radio interface unit is a control device, which controls the elements that are connected to it, it would have been obvious to one of ordinary skill in the art at the time of invention to modify the Phillips' radio/antenna interface unit as suggested by Fischer to include the registers inside the radio interface device in order to save the control information of the other units. Fischer is silent in disclosing that the registers are memory-mapped registers, however since the memory-mapped registers have the fastest mechanism for data retrieval (e.g. as evidence by Santos et al.[1]), it would have been obvious to one of ordinary skill in the art at the time of invention to use these kind of registers instead of the registers used by Fischer for the reasons stated above. Philips, park and Fischer disclose all the subject matters claimed in claims 1, 12, and 13, except that the memory-mapped registers configured to control data generated by the bus processor. Yarch discloses a system wherein a PCI bus interface and the local bus interface can be programmed from the local bus through a memory-mapped register (see column 4, lines 4-6). It would have been obvious to one of ordinary skill in the art at the time of invention to modify Philips, park and Fischer, as suggested by Yarch to use only one bus for reading and writing purposes from and to the memory and reduce cost of the system.

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[1] Santos et al. (US 5,933,158, see column 24, first paragraph)

As to claim 27, Philips, park and Fischer disclose all the subject matters claimed in claims 23, except that the memory-mapped registers configured to control data generated by the bus processor. Yarch discloses a system wherein a PCI bus interface and the local bus interface can be programmed from the local bus through a memory-mapped register (see column 4, lines 4-6). It would have been obvious to one of ordinary skill in the art at the time of invention to modify Philips, park and Fischer, as suggested by Yarch to use only one bus for reading and writing purposes from and to the memory and reduce cost of the system.

As to claims 3 and 14, Fischer further discloses that the radio interface unit 402 includes a state machine equipped to access the registers (see Fig. 3). It would have been obvious to one of ordinary skill in the art at the time of invention to use a radio interface unit as suggested by Fischer including a state machine having access to the register sets to provide the appropriate signals to the other parts of the system (see column 5, lines 4-6).

As to claims 4 and 15, Fischer discloses that the radio interface 402 includes a processor interface (the state machine 404 has been interpreted as processor interface) for accessing the register. It would have been obvious to one of ordinary skill in the art at the time of invention to use a radio interface unit as suggested by Fischer including a state machine (or processor interface) having access to the register sets to provide the appropriate signals to the other parts of the system (see column 5, lines 4-6).

As to claims 6 and 17, Phillips further discloses a clock, coupled to the RIP, for determining the relative timing of external events, and also for controlling the analog radio module (See column 14, lines 35-49).

As to claims 9 and 20, Philips discloses that the RIP accessed controlling software that is programmed according to one or more specific electronic characteristics of a given analog audio module (see column 25, lines 14-20).

As to claims 10 and 21, Park discloses that the nonlinearities include at least one of AGC (automatic gain control) line voltage as a function of gain, and power level control voltage as a function of power output (See Fig. 3, blocks 217 and 223, and column 6, lines 49-51), whereby the digital module need not be modified to work with the specific characteristics of a given analog radio module (i.e. the analog signal nonlinearities have been compensate before the transmission of signal to the digital form) (see Figs. 5 and 6).

As to claim 11 and 22, Phillips discloses that the digital module is a time-division-duplex (see column 23, lines 8 and Fig. 1 for duplexing), user-equipment (See column 7, lines 47-55), application-specific-integrated-circuit (ASIC) (see column 14, lines 50-67).

As to claim 28, Fischer further discloses that the radio interface unit 402 includes a state machine equipped to access the registers (see Fig. 3). It would have been obvious to one of ordinary skill in the art at the time of invention to use a radio interface unit as suggested by Fischer including a state machine having access to the register sets to provide the appropriate signals to the other parts of the system (see column 5,

lines 4-6). Philips, park and Fischer disclose all the subject matters claimed in claims 28, except that the memory-mapped registers configured to control data generated by the bus processor. Yarch discloses a.system wherein a PCI bus interface and the local bus interface can be programmed from the local bus through a memory-mapped register (see column 4, lines 4-6). It would have been obvious to one of ordinary skill in the art at the time of invention to modify Philips, park and Fischer, as suggested by Yarch to use only one bus for reading and writing purposes from and to the memory and reduce cost of the system.

As to claim 29, Fischer discloses that the radio interface 402 includes a processor interface (the state machine 404 has been interpreted as processor interface) for accessing the register. It would have been obvious to one of ordinary skill in the art at the time of invention to use a radio interface unit as suggested by Fischer including a state machine (or processor interface) having access to the register sets to provide the appropriate signals to the other parts of the system (see column 5, lines 4-6).

7. Claims 5, 16, 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Phillips, Park, and Fischer, and Yarch, further in view of Bhandal et al. (hereafter, referred as Bhandal) (US 6,532,533).

As to claims 5, 16, and 30 Phillips, Park, Fischer, and Yarch disclose all the subject matters claimed in claims 3, 14, and 28 except that the radio interface includes one or more GPIO registers for accessing the memory-mapped registers. Bhandal discloses a processing device which provides general-purpose input/output pins for use by software routines as needed (see the abstract). Bhandal further discloses that

GPIO pins are driven or monitored by reading or writing to a set of memory mapped registers (see column 4, lines 27-34). It would have been obvious to one of ordinary skill in the art at the time of invention to use the method taught by Bhandal to simplify the system (see column 2, lines 25-35).

Allowable Subject Matter

8. Claims 8, 19, and 33 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leila Malek whose telephone number is 571-272-8731. The examiner can normally be reached on 9AM-5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on 571-272-3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Leila Malek
Examiner
Art Unit 2611

L.M.

MOHAMMED GHAYOUR
SUPERVISORY PATENT EXAMINER